

IN THE CLAIMS:

Please cancel claims 10 and 15, without prejudice.

Please amend claims 11, 16, and 17 in "clean" format, as follows:

Sub D1
CX

11. (Twice Amended) A semiconductor integrated circuit comprising:
a pad to which an input signal is externally input;
a source follower circuit including a transistor having a gate connected to said pad and a source for producing an output signal;
wherein a parasitic capacitance is created between said pad and a semiconductor substrate, and said source of the source follower circuit is connected to the semiconductor substrate side of the parasitic capacitance so as to charge and discharge the parasitic capacitance by the output signal of said source follower circuit;
an island region on the upper surface of said semiconductor substrate containing impurities of a second conductivity type, and the pad formed on said island region via an oxide film; and wherein said semiconductor substrate contains impurities of a first conductivity type; and wherein an output terminal of said source follower circuit is connected to said island region.

C2

16. (Amended) The semiconductor integrated circuit defined in Claim 11, wherein said source follower circuit comprises an amplifier.

17. (Amended) The semiconductor integrated circuit defined in Claim 11, wherein said source follower circuit comprises a field effect transistor integrated on said semiconductor substrate, said field effect transistor having a gate connected to said pad.

Please add claims 19-20, as follows:

C3

19. (Newly Added) A method of reducing an attenuation of an input signal to a junction field-effect transistor, the method comprising controlling a charging amount of a parasitic capacitance by changing the input signal.

Cond Sub D1

20. (Newly Added) The method of claim 19, wherein controlling said magnitude of said parasitic capacitance further comprising connecting a source follower circuit to a pad and connecting an output terminal of said source follower circuit to an island region disposed between said pad and a semiconductor substrate.